SYSTEM AND METHOD FOR DYNAMIC CLOCK GENERATION

ABSTRACT OF THE DISCLOSURE

An application specific integrated circuit (ASIC) has a clock controller that dynamically selects an appropriate clock frequency for a resource. The ASIC includes a central processing unit (CPU), on-chip memory, a memory controller controlling external memory devices, a system bus, and various peripheral controllers. Devices that can be accessed by other devices, such as the on-chip memory, the memory controller, and the system bus are "resources." The devices that access the resources are "controllers." The ASIC generates a master clock and the clock controller derives clocks for driving the resources and controllers from the master clock. A multiplexer (MUX) in the clock controller selects the clock that is passed to a resource. Each controller has a request line to the clock controller for signaling when the controller is accessing a resource. The clock controller has a programmable register for each controller holding a value representing the bandwidth utilization of the controller and an adder and a frequency table. The adder sums the contents of the bandwidth registers of the controllers that are accessing a resource. The sum is an index to an entry in a frequency table. The value held in the frequency table is applied to the selection inputs of the MUX to select the clock for the resource. If no controllers are requesting access to the memory controller, the clock controller shuts down the memory clock. Accordingly, the clock frequency of the resource is determined by the bandwidth utilization of the controllers requesting access to the resource.